

LATCH and DRIVER for FIP
CMOS LSI**DESCRIPTION**

The μ PD6323AC is a latch and driver CMOS IC for FIP (Fluorescent Indicator Panel). For multiplex wiring, the μ PD6323AC is supplied with the serial interface circuit, 21 bit shift register, 21 bit data latch and 21 outputs. The serial data transfer from the data source to the μ PD6323AC is accomplished with 3 signals.

FEATURES

- Direct Connection to Battery enable.
- Wide Supply Voltage $V_{DD} = 8$ to 14 (V)
- Serial Input 21 bit Shift Register Incorporated.
- Data Control by Transmission Clock (External) and Latch.
- Suitable for Static Display by Buffer Register.
- Brightness Control Enable: External Duty Control.
- Output Characteristics $V_{out} = 40$ V.
 $I_{out} = 5$ mA.
- 28 Pin Plastic Molded DIP (Dual In-line Package).
- Serial Interface Format: Compatible with NEC microcomputer.

ABSOLUTE MAXIMUM RATINGS (T_a = 25 ± 2 °C)

Supply Voltage at V _{DD} terminal	V _{DD}	18	V
Input Voltage	V _{IN}	-0.3 to V _{DD}	V
Output Voltage (3 to 13, 16 to 25 Pins)	V _{O0} to V _{O20}	-40 (*1)	V
Output Current (3 to 13, 16 to 25 Pins)	I _{O0} to I _{O20}	-5	mA
Operating Temperature Range	T _{opt}	-40 to +85	°C
Storage Temperature Range	T _{stg}	-55 to +125	°C

Notes: (*1): These Voltage are referenced to the V_{DD}.

RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Operating Temperature Range	T _{opt}	-40		+85	°C
Operating Supply Voltage	V _{DD}	8		14	V
Output Voltage (3 to 13, 16 to 25 Pins) (*2)	V _{O0} to V _{O20}		-19	-35	V
Output Current (3 to 13, 16 to 25 Pins)	I _{O0} to I _{O20}		-2	-5	mA
Input Voltage High	V _{IH}	3.5		V _{DD}	V
Input Voltage Low	V _{IL}	V _{SS}		1.0	V
SCK Frequency	f _{SCK}			500	KHz
SCK Cycle Time (*3)	t _{KCY}	2.0			μs
SCK High Level Pulse Width (*3)	t _{KHW}	0.9			μs
SCK Low Level Pulse Width (*3)	t _{KLW}	0.9			μs
SI Setup Time to SCK ↑ (*3)	t _{SIK}	0.4			μs
SI Hold Time (*3)	t _{KSI}	0.4			μs
SCK → LH Valid Time (*4)	t _{CLL}	1.8			μs
LH High Level Pulse Width (*4)	t _{LHW}	1.8			μs
BI High Level Pulse Width (*5)	t _{BHW}	0.4			μs

Notes: (*2): These Voltage are referenced to the V_{DD}.

(*3): See Fig. 1

(*4): See Fig. 2

(*5): See Fig. 3

ELECTRICAL CHARACTERISTICS (Recommended operating conditions)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Input Leakage Current	I_{IL}			± 10	μA	$V_{IN} = V_{SS}$ or $V_{IN} = V_{DD}$
SO Output Voltage High	V_{SOH}	$V_{DD}-1$		V_{DD}	V	$I_{SOH} = -1$ mA
SO Output Voltage Low	V_{SOL}	V_{SS}		0.5	V	$I_{SOL} = 1$ mA
Output Voltage High (3 to 13, 16 to 25 Pins)	V_O	$V_{DD}-1.5$		V_{DD}	V	$I_O = -5$ mA O_0 to O_{20} Output
Output Leakage Current (3 to 13, 16 to 25 Pins)	I_{OLL}			10	μA	V_{DD} to $V_O = 40$ V
Supply Current at V_{DD} Terminal	I_{DD}			2	mA	All Input = [High] All Output = Open
Supply Voltage at V_{DD} Terminal to Keep DATA	$V_{DD}(H)$	3.0			V	Drop V_{DD} on latch DATA (MIN.)
Input Capacitance	C_{IN}			15	pF	$f = 1$ MHz
$\overline{SCK} \rightarrow SO$ Valid Time (*6)	t_{KSO}			0.5	μs	
$BI \rightarrow Q_n$ Valid Time (*5)	t_{BKQ}			1.8	μs	

Note: (*6); See Fig. 4

TIMING CHART

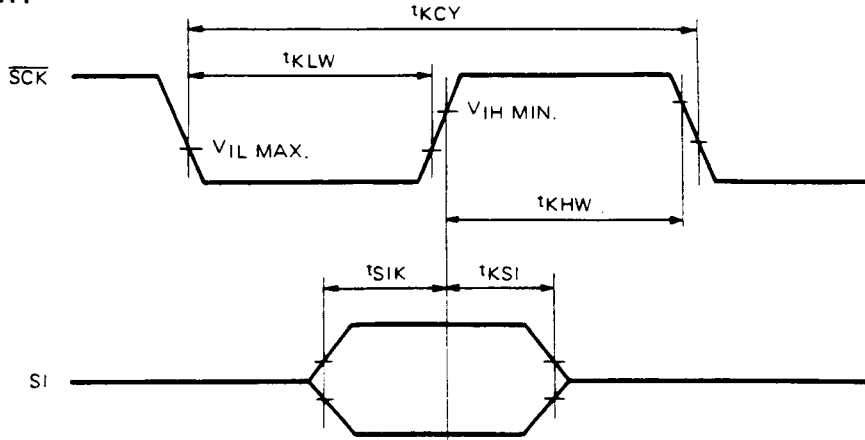


Fig. 1

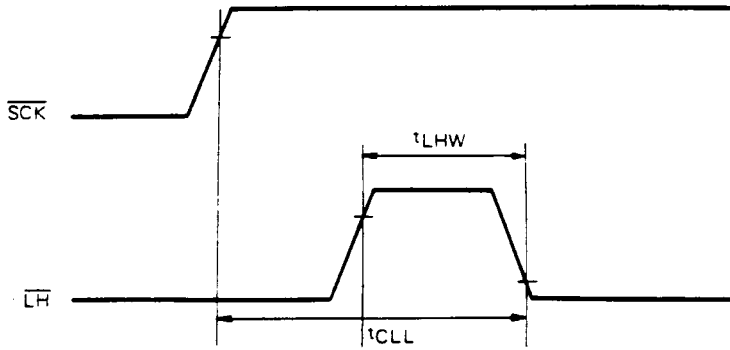


Fig. 2

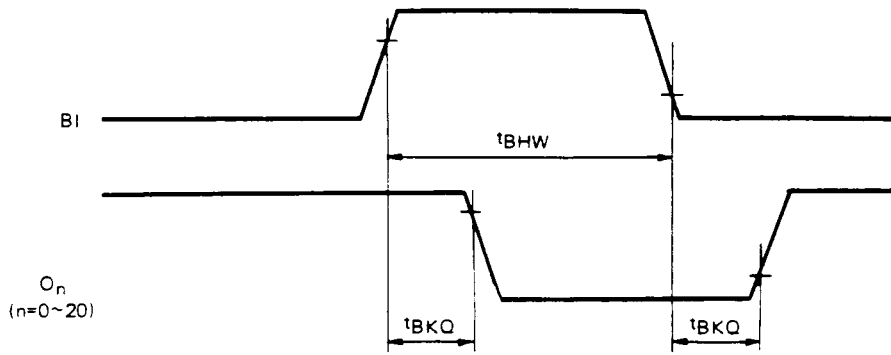


Fig. 3

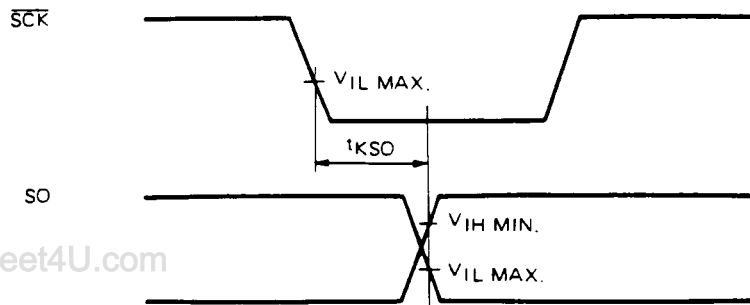
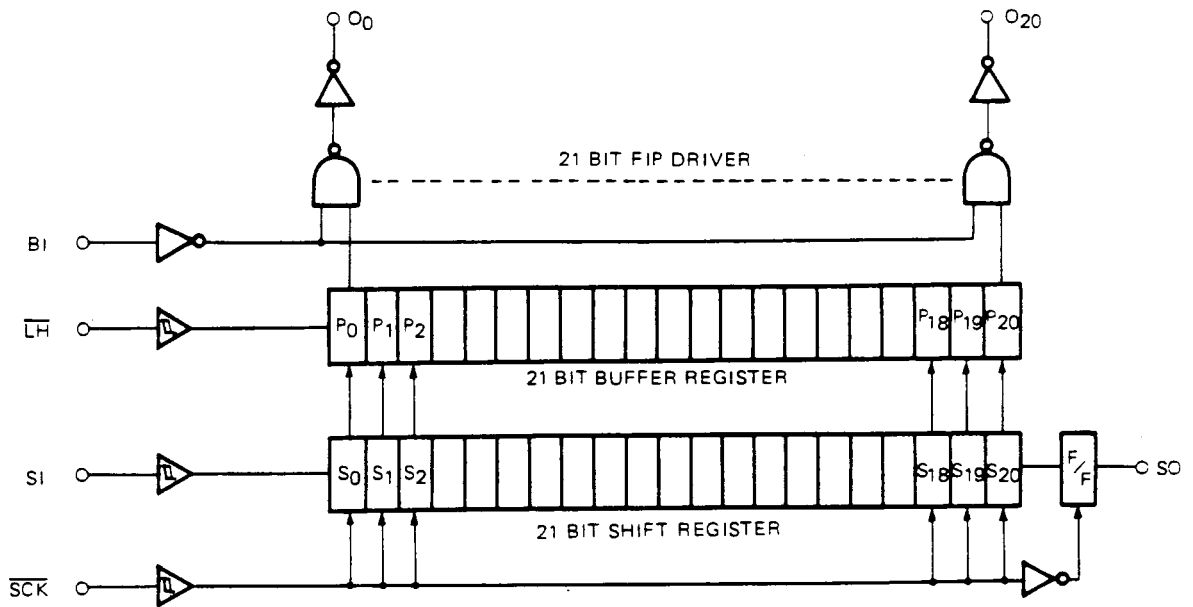
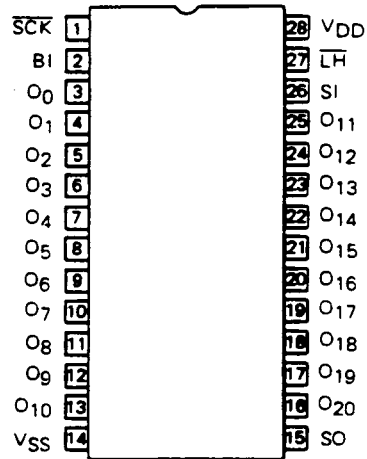


Fig. 4

BLOCK DIAGRAM



PIN CONNECTION (Top View)

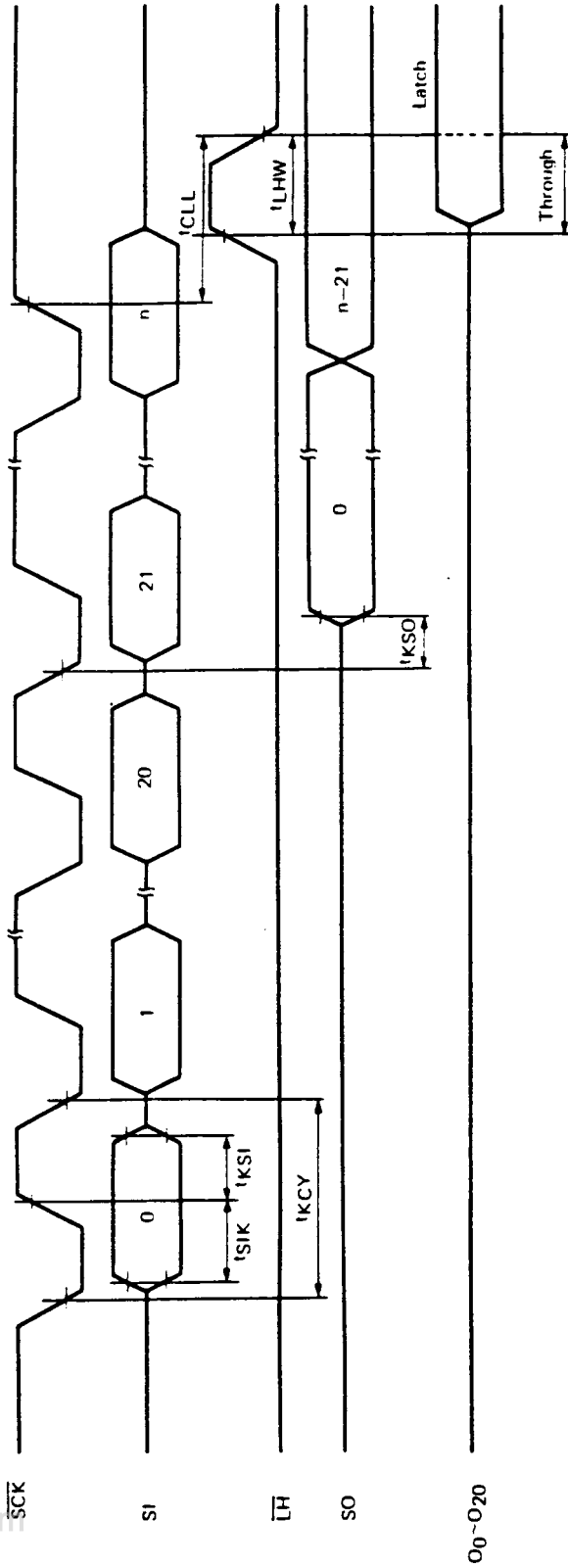


FUNCTION

PIN NUMBER	SYMBOL	FUNCTION	INPUT/ OUTPUT	EXPLANATION
1	\overline{SCK}	Serial Clock Input	INPUT	The SI data are read and stored in the 21 bit shift register at the rising edge of \overline{SCK} . DATA output from SO at the dropping edge of \overline{SCK} .
2	BI	Blanking Input	INPUT	When "L" level signal is supplied to the BI, O ₀ to O ₂₀ are active. "H": O ₀ to O ₂₀ are disable. Dimmer function is possible by external duty control.
3	O ₀	Segment and Driver for FIP (O ₀ to O ₁₀)	OUTPUT	Outputs are, Pch MOS Open Drain. These 11 Output are the Outputs of 11 bit output data latch, which can drive FIP directly.
4	O ₁			
5	O ₂			
6	O ₃			
7	O ₄			
8	O ₅			
9	O ₆			
10	O ₇			
11	O ₈			
12	O ₉			
13	O ₁₀			
14	V _{SS}	GND		Connection to GND.
15	SO	Serial data Output	OUTPUT	Serial data output at the dropping edge of \overline{SCK} . In case of "n" pieces of μ PD6323AC are serial connected, so it is possible to connect one to next SI.
16	O ₂₀	Segment and driver for FIP (O ₁₁ to O ₂₀)	OUTPUT	Outputs are, Pch MOS Open Drain. These 10 outputs are the Outputs of 10 bit output data latch, which can drive FIP directly.
17	O ₁₉			
18	O ₁₈			
19	O ₁₇			
20	O ₁₆			
21	O ₁₅			
22	O ₁₄			
23	O ₁₃			
24	O ₁₂			
25	O ₁₁			
26	SI	Serial data Input	INPUT	Serial Data Input. The SI data are read and stored in the 21 bit shift register at the rising edge of \overline{SCK} .

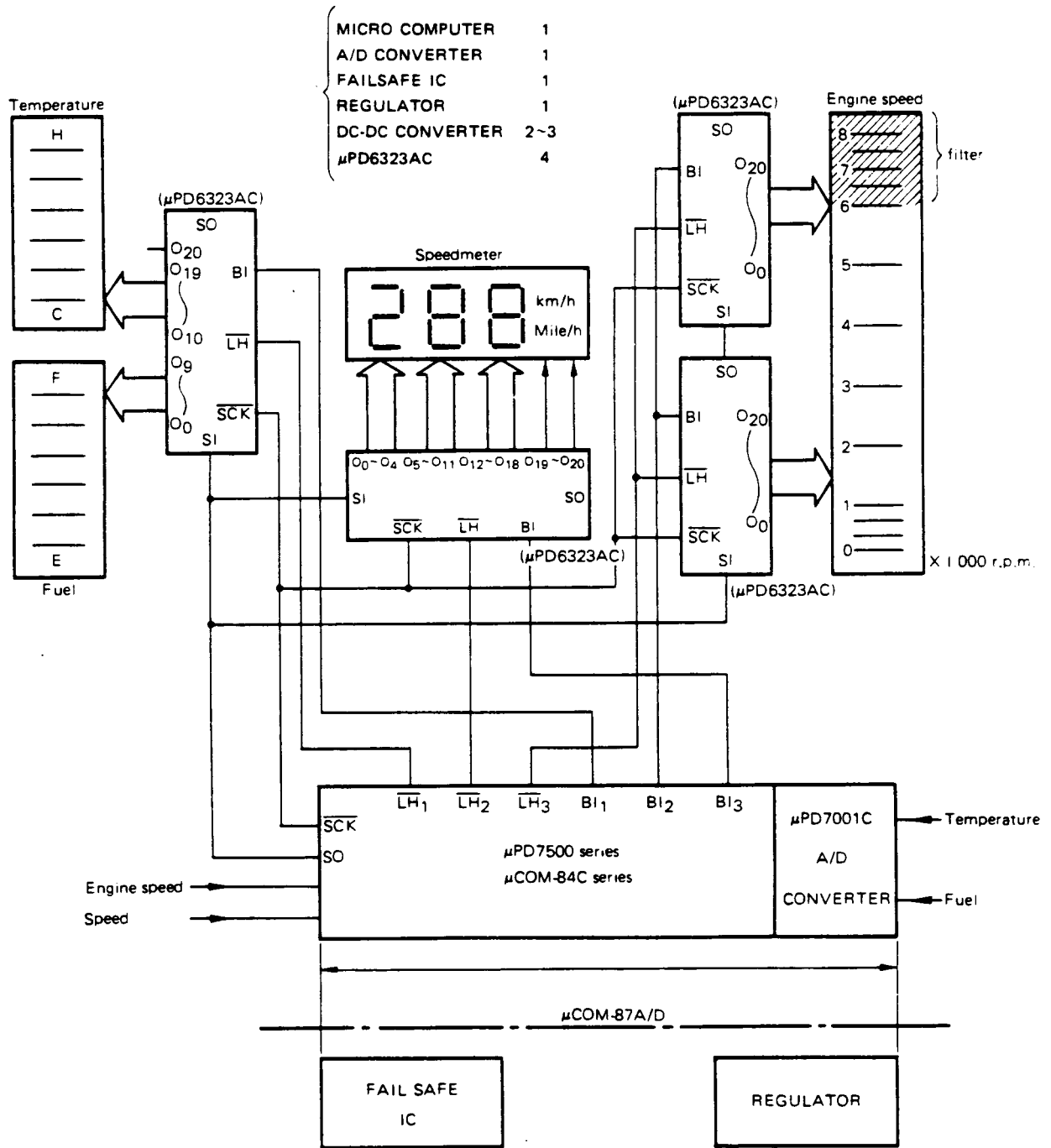
PIN NUMBER	SYMBOL	FUNCTION	INPUT/ OUTPUT	EXPLANATION
27	$\overline{\text{LH}}$	Latch and Hold Input	INPUT	When "H" level signal is supplied to the $\overline{\text{LH}}$, the data of 21 bit shift register are normally transferred to the 21 bit output data latch. At the time of the rising edge of $\overline{\text{LH}}$; the data of 21 bit output data latch are hold. "L"; The data of 21 bit output data latch are protected.
28	V_{DD}	Supply Voltage at V_{DD} terminal		$V_{\text{DD}} = 8 \text{ to } 14 \text{ (V)}$

TIMING CHART



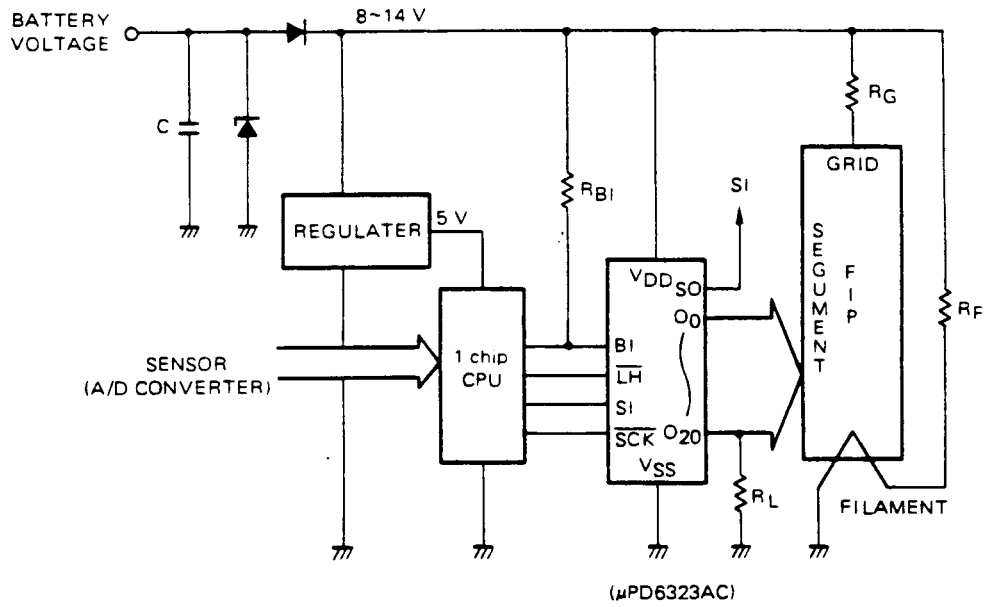
APPLICATION CIRCUIT

(1) AUTOMOTIVE DASHBOARD SYSTEM SYSTEM CONSTRUCTION

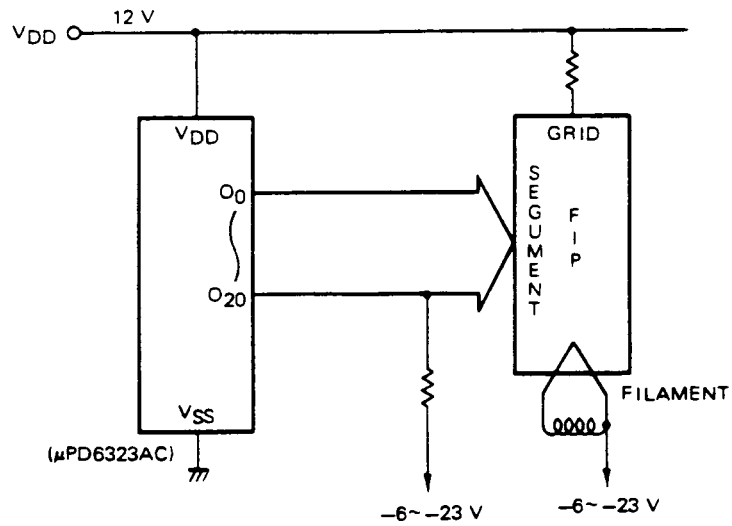


Each data of Engine speed, speed, temperature and fuel is divided to each group by $\overline{\text{LH}}$ control.
 Each data is transferred by SI and $\overline{\text{SCK}}$ control.
 FIP dimmer control is capable by BI's duty control.

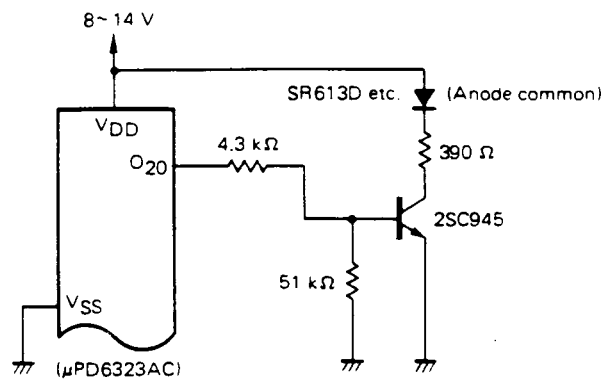
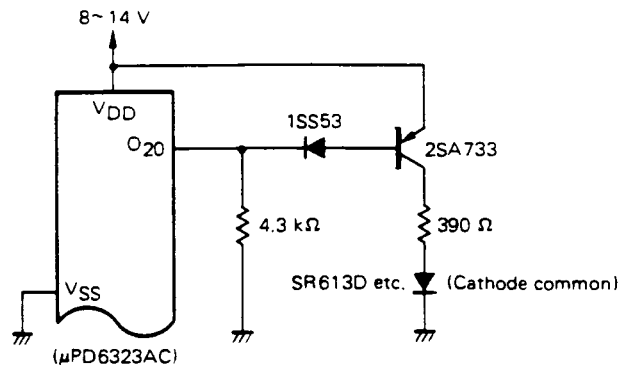
(2) 12 V FIP DRIVER CIRCUIT



(3) HIGH VOLTAGE (18 to 35 V) FIP DRIVER CIRCUIT



(4) LED DRIVER CIRCUIT



(5) EXAMPLE OF SOFTWARE

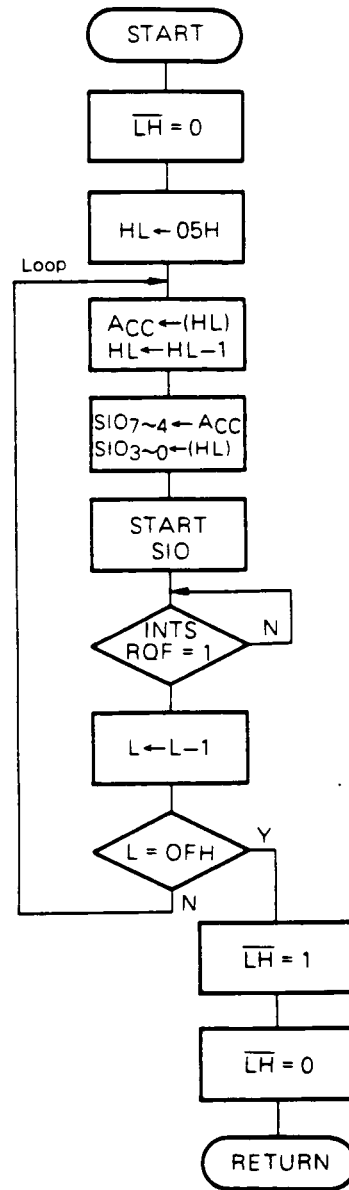
Using of serial I/O of μ -COM 75 series
Subroutine of 24 bit data transfer

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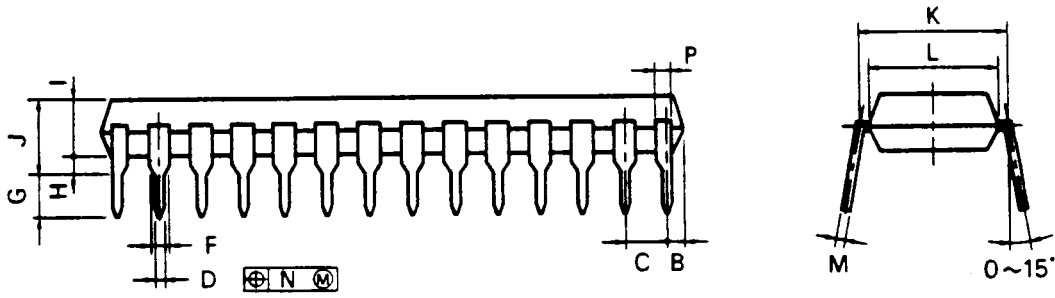
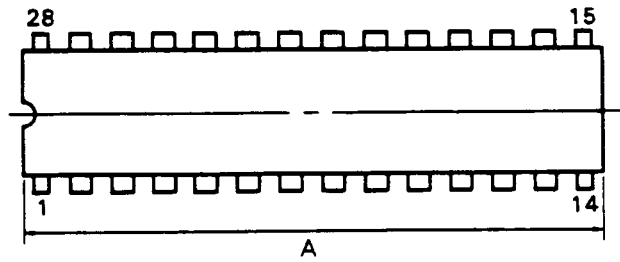
SI OUT : ANP  6,7
        LHLI 05H
LOOP   : LAM  HL-
        TAMSIO
        SIO
        SKI  2
        JCP  $-2
        DLS
        JCP  LOOP
        ORP  6,8
        ANP  6,7
        RT
    
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RAM (ADD)	TRANSFER BIT			
	3	2	1	0
00H	O ₃	O ₂	O ₁	O ₀
01H	O ₇	O ₆	O ₅	O ₄
02H	O ₁₁	O ₁₀	O ₉	O ₈
03H	O ₁₅	O ₁₄	O ₁₃	O ₁₂
04H	O ₁₉	O ₁₈	O ₁₇	O ₁₆
05H	O ₂₃	O ₂₂	O ₂₁	O ₂₀

Allot port
P₆₃- $\overline{\text{LH}}$



28PIN PLASTIC DIP (400 mil)



P28C-100-400

NOTES

- 1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.
- 2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	35.56 MAX.	1.400 MAX.
B	1.27 MAX.	0.050 MAX.
C	2.54 (T.P.)	0.100 (T.P.)
D	0.50 ^{+0.10}	0.020 ^{+0.004}
F	1.1 MIN.	0.043 MIN.
G	3.5 ^{+0.3}	0.138 ^{+0.012}
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.72 MAX.	0.226 MAX.
K	10.16 (T.P.)	0.400 (T.P.)
L	8.6	0.339
M	0.25 ^{+0.08}	0.010 ^{+0.003}
N	0.25	0.01
P	0.9 MIN.	0.035 MIN.